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SILICON-ON-SAPPHIRE MATERIAL AND DEVICE PROPERTIES AT HIGH AND LOW TEMPERATURE

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Silicon On Sapphire (SOS) technology has recently undergone significant improvements in terms of crystal quality, wafer size (8") and film thicknesses (50-100nm). As compared to modern Silicon On Insulator (SOI) materials such as SIMOX, Unibond, etc, SOS was handicapped mainly by low-volume production, stress effects affecting the carrier mobility and poor quality of Si/Al_2O_3 interface [1]. However, SOS features key properties which should not be disregarded:

- Fully insulating Al_2O_3 substrate, which reduces microwave losses and makes SOS be an ideal candidate for the integration of RF circuits for wireless communi cation [2].
- High thermal conductivity of sapphire which allows thermal dissipation through the substrate and alleviates self-heating effects [3].
- Low carrier lifetime, leading to reduced gain of parasitic bipolar transistor and therefore improved breakdown voltage of CMOS circuits [4].

The aim of this paper is to present a thorough examination and update the electrical properties of recent silicon on sapphire wafers.

Initial material evaluation was conducted on bare SOS wafers with 100 nm Si film. Van der Pauw samples were prepared and Hall-effect measurements were performed, at low and high temperature, in order to determine volume carrier mobility and residual doping level in the Si film. The results will be discussed according to two different hypothesis: (a) rather homogenous film with 'volume' conduction, and (b) high density of interfacial defects resulting in the natural build-up of an accumulation channel at the Si/Al_2O_3 interface.

In order to correlate material properties with device performances, the static and dynamic behaviour of CMOS transistors were investigated in a wide range of temperature (from 20 K to 500 K). Fully depleted NMOS and PMOS SOS transistors with T-gate and various lengths (L=0.3 to 5μm) and widths (W=50,100,200μm) were tested. Electrical parameters (mobility, density of states, doping level, carrier lifetime) were extracted and compared with those of bulk-Si and other SOI materials.

Well behaved drain current $I_D(V_G)$ and transconduc tance $g_m(V_G)$ characteristics (Fig. 1) were obtained in both NMOS and PMOS transistors. The influence of the edge transistor, observed for the n-channels, is reinforced when temperature is lowered; this result suggests that the temperature variation of the threshold voltage on the edge transistors is lower than at the front channel.

$I_D/\sqrt{g_m}$ versus gate voltage plots allow extracting the threshold voltage, V_T, and the mobility. The variation rate of V_T when the temperature is reduced is about 0.2mV/°C for NMOSFETs (Fig. 2). At room temperature the hole (μ_p) and electron (μ_n) mobilities are reasonable. Our measurements show that the carrier mobility increases at low temperature more rapidly for holes than for electrons. This result can be explained by the difference in doping level between n- and p-channels. The subthreshold slope (Fig. 2) linearly decreases when the temperature is lowered from 300 K to 100 K.

Additional dynamic measurements permit to estimate the carrier lifetime in the silicon film. Drain current overshoots and undershoots are obtained when turning-on or -off the transistor. It was found that the transient duration is reduced when increasing the temperature, while the carrier lifetime augments.

In conclusion, SOS technology offers new attributes for the fabrication of integrated circuits, being very well suited for circuits operating in microwave range.

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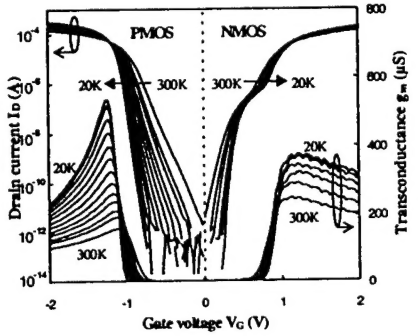
Fig. 1. Experimental drain current I_D (semi-log scale) and



transconductance g_m versus gate voltage in SOS NMOS and PMOS transistors for different temperatures (L=1μm, V_D=100mV).

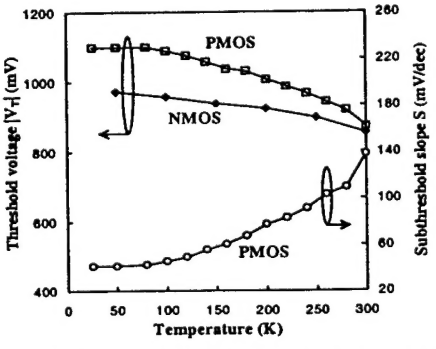


Fig. 2. Dependence of threshold voltage and subthreshold slope on temperature (L=1μm).